

Parasitic Effects

Parasitic Capacitance & SRF

Real inductors have parasitic capacitance between turns and layers that limits their useful frequency range. Understanding these effects is critical for VIC design, as they determine the maximum operating frequency and affect circuit tuning.

Sources of Parasitic Capacitance

Parasitic capacitance in inductors comes from several sources:

1. Turn-to-Turn Capacitance (C_{tt})

Capacitance between adjacent turns in the same layer. Depends on wire spacing and insulation.

2. Layer-to-Layer Capacitance (C_{ll})

Capacitance between winding layers. Often the largest contributor in multi-layer coils.

3. Winding-to-Core Capacitance (C_{wc})

Capacitance between the winding and the magnetic core (if conductive or grounded).

4. Winding-to-Shield Capacitance

In shielded inductors, capacitance to the external shield.

Self-Resonant Frequency (SRF)

The parasitic capacitance resonates with the inductance at the Self-Resonant Frequency:

$$SRF = 1 / (2\pi\sqrt{L \times C_{parasitic}})$$

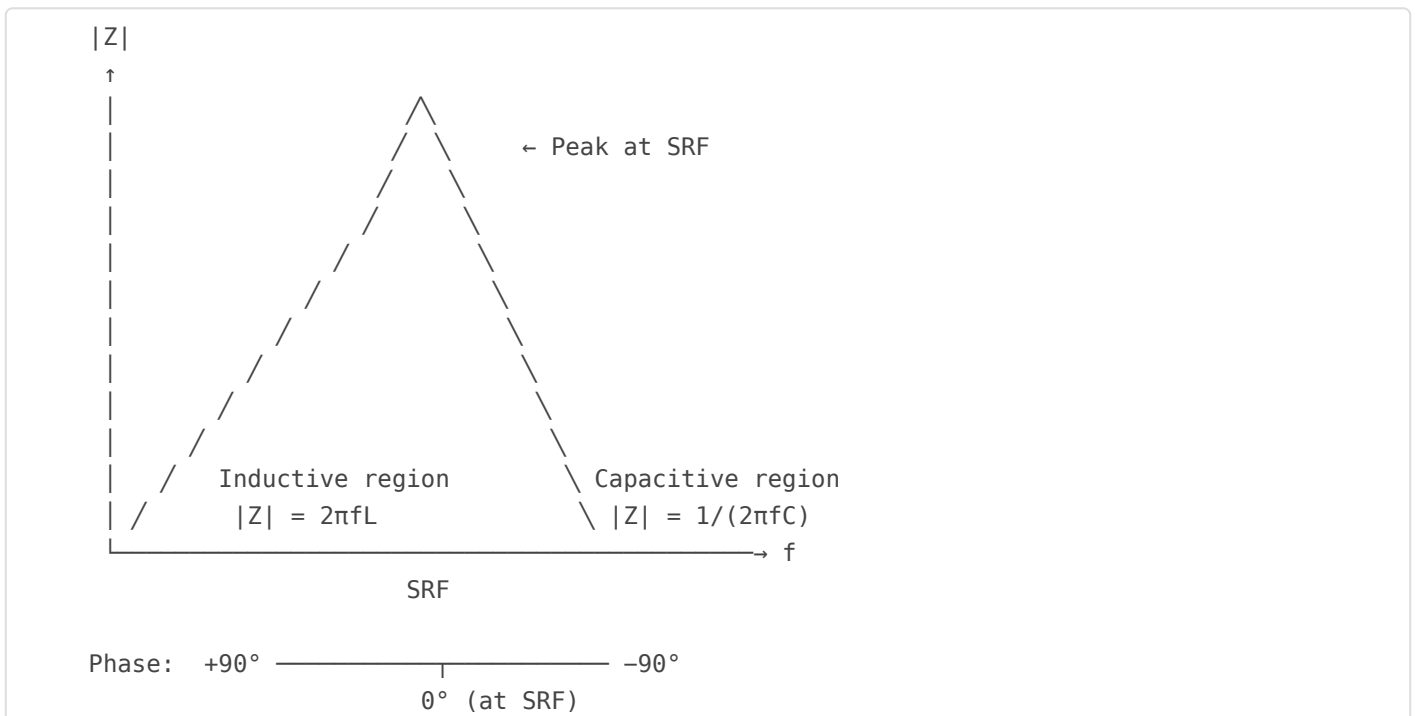
Behavior at SRF:

- Impedance is maximum (parallel resonance)
- Inductor is neither inductive nor capacitive
- Phase angle crosses through 0°

Above SRF:

The "inductor" behaves as a **capacitor**! Impedance decreases with frequency.

Impedance vs. Frequency



Operating Frequency Guidelines

f_{op} / SRF	Behavior	Recommendation
< 0.1 ($< 10\%$)	Nearly ideal inductor	Preferred range
$0.1 - 0.3$ (10-30%)	Slight inductance increase	Acceptable with correction

f_{op} / SRF	Behavior	Recommendation
0.3 - 0.7 (30-70%)	Significant deviation	Caution - Q drops
> 0.7 (> 70%)	Near or past SRF	Do not use

Effective Inductance Near SRF

As frequency approaches SRF, the apparent inductance increases:

$$L_{eff} = L_{dc} / [1 - (f/SRF)^2]$$

Example:

- $L_{dc} = 10 \text{ mH}$, $SRF = 100 \text{ kHz}$
- At 30 kHz: $L_{eff} = 10 / [1 - 0.09] = 11.0 \text{ mH}$ (+10%)
- At 50 kHz: $L_{eff} = 10 / [1 - 0.25] = 13.3 \text{ mH}$ (+33%)
- At 70 kHz: $L_{eff} = 10 / [1 - 0.49] = 19.6 \text{ mH}$ (+96%)

Minimizing Parasitic Capacitance

Winding Techniques:

1. **Single-layer winding:** Eliminates layer-to-layer capacitance
2. **Space-wound turns:** Increases turn-to-turn distance
3. **Honeycomb/basket winding:** Crosses turns to reduce adjacent voltage
4. **Bank winding:** Winds in sections to reduce voltage across layers
5. **Progressive winding:** Keeps voltage gradient low between adjacent turns

Design Choices:

- Use fewer turns (requires higher permeability core)
- Use thinner insulation (but watch voltage ratings)
- Use air-core (eliminates winding-to-core capacitance)
- Choose toroidal cores (natural progressive winding)

Calculating Parasitic Capacitance

Turn-to-Turn Capacitance (Simplified)

$$C_{tt} \approx \epsilon_r \times l_{turn} \times d_{wire} / s$$

Where s is the spacing between adjacent turn centers.

Layer-to-Layer Capacitance

$$C_{ll} \approx \epsilon_r \times A_{layer} / t_{insulation}$$

Where A_{layer} is the overlapping area between layers.

Total Parasitic Capacitance

The total equivalent capacitance is complex because the distributed capacitances see different voltages. For a rough estimate:

$$C_{parasitic} \approx C_{ll}/3 + C_{tt}/N$$

The 1/3 factor accounts for voltage distribution across layers.

Measuring SRF

Method 1: Impedance Analyzer

1. Connect inductor to impedance analyzer
2. Sweep frequency and plot $|Z|$
3. SRF is where impedance peaks

Method 2: Signal Generator + Oscilloscope

1. Connect inductor in series with known resistor
2. Drive with sine wave, sweep frequency
3. Monitor voltage across inductor
4. SRF is where voltage peaks (current minimum)

Method 3: Resonance with Known Capacitor

1. Measure inductance at low frequency
2. Add known capacitor in parallel
3. Find new resonant frequency
4. Calculate parasitic C from the difference

SRF in VIC Design

Problem	Symptom	Solution
Operating too close to SRF	Resonance frequency higher than calculated	Reduce tuning cap or use different choke
Operating above SRF	No resonance, circuit acts capacitive	Must redesign with fewer turns
Low SRF in bifilar winding	Limited usable frequency range	Accept limitation or use separate chokes

VIC Matrix Calculator: The Choke Design module estimates SRF based on winding geometry and displays a warning if your operating frequency is too close to SRF. It also calculates the effective inductance at your operating frequency.

Next: DC Resistance and Q Factor →

Revision #1

Created 2026-01-01 20:42:08 UTC by Chris Bake

Updated 2026-01-01 20:42:17 UTC by Chris Bake