PLL Control

PLL-Based Frequency Control

Phase-Locked Loop (PLL) circuits can automatically track and maintain resonance in VIC systems, compensating for drift due to temperature changes, water level variations, and other factors. This page covers PLL fundamentals and their application to VIC circuits.

Why PLL Control?

VIC resonant frequency can drift during operation due to:

Factor	Effect on f_0	Typical Drift
Water temperature rise	f_0 increases (ε_r drops)	+0.2%/°C
Gas bubble formation	f_0 increases (C drops)	+2-10%
Water level change	f_0 changes (C changes)	Variable
Core temperature rise	f_0 may shift (μ changes)	±1%

A PLL can continuously adjust the drive frequency to maintain optimal resonance despite these variations.

PLL Fundamentals

Basic PLL Components:

```
Reference ──→ [Phase      ] ──→ [Loop    ] ──→ [VCO     ] ──→ Output
Signal        [Detector   ]     [Filter  ]     [        ]     Frequency
                   ↑                                 |
                   └─────────────────────────────────┘
                             Feedback
```

Components Explained:

- **Phase Detector:** Compares phase of two signals, outputs error voltage
- **Loop Filter:** Averages error signal, sets response speed
- **VCO:** Voltage-Controlled Oscillator, frequency varies with input voltage

PLL for VIC Resonance Tracking

For VIC applications, the PLL tracks the resonant frequency by sensing the phase relationship between drive signal and cell response:

```
             ┌──────────────────────────────────────────┐
             │                                          │
Drive ──→ [VIC Circuit] ──→ Vwfc ──→ [Phase    ] ──→ [Loop   ] ──→ [VCO]
Signal                              [Detector ]     [Filter ]        │
  ↑                                      ↑                           │
  └──────────────────────────────────────┴───────────────────────────┘
                                Feedback Loop
```

Phase Detection Methods

Method	Description	Pros/Cons
XOR Phase Detector	Digital XOR of drive and response	Simple, but needs square waves
Analog Multiplier	Multiply drive × response	Works with sinusoids, more complex
Zero-Crossing Detector	Compare zero-crossing times	Digital-friendly, noise sensitive
I/Q Demodulation	Quadrature phase detection	Most accurate, most complex

Resonance Tracking Logic

At resonance, the phase relationship between drive current and WFC voltage is 0°:

Phase vs. Frequency:

> > - **$f < f_0$:** V leads I (capacitive), phase > 0°
> > - **$f = f_0$:** V and I in phase, phase = 0°
> > - **$f > f_0$:** V lags I (inductive), phase < 0°

Control Law:

> - If phase > 0°: Increase frequency (move toward resonance)
> - If phase < 0°: Decrease frequency (move toward resonance)
> - If phase ≈ 0°: Maintain frequency (at resonance)

Loop Filter Design

The loop filter determines how quickly the PLL responds to changes:

Parameter	Fast Response	Slow Response
Tracking speed	Quick adaptation	Slow adaptation
Noise rejection	Poor	Good
Stability	May oscillate	More stable
Best for	Rapid changes	Gradual drift

Design Tip: For VIC applications, a medium-speed loop (bandwidth ~100-500 Hz) usually works well. Fast enough to track bubble-induced changes, slow enough to reject noise.

VCO Implementation

The VCO generates the variable-frequency drive signal:

Common VCO Options:

- **555 Timer VCO:** Simple, wide frequency range, moderate stability
- **74HC4046 PLL IC:** Integrated PLL with VCO, easy to use
- **DDS (Direct Digital Synthesis):** Precise frequency control, programmable
- **Microcontroller PWM:** Software-adjustable, flexible

VCO Requirements:

- Frequency range covering expected f_0 ± drift range
- Linear frequency vs. voltage response
- Low noise and jitter
- Fast frequency settling

Complete PLL-VIC System

```
                    PLL CONTROLLER
    ┌─────────────────────────────────────────┐
    │                                         │
    │  [Phase Det] ──→ [Loop Filter] ──→ Vctrl│
    │       ↑                            │    │
    │       │                            │    │
    └───────┼────────────────────────────┼────┘
            │                            │
            │                            ↓
   Vsense   │                          [VCO]
     ↑      │                            │
     │      │                            ↓
     │      │                      [Driver Stage]
     │      │                            │
     │      │      ┌─────────────────────┘
     │      │      ↓
     │      └── [L1] ──── [C1] ─────────┐
     │                                  │
     │          ┌───────────────────────┘
     │          │
     │          ↓
     └───── [L2] ──── [WFC]
```

```
                ↑
         Resonating
           Circuit
```

Practical Considerations

Startup Sequence:

1. Initialize VCO near expected f_0
2. Enable PLL with wide bandwidth initially
3. Wait for lock indication
4. Reduce bandwidth for stable operation

Lock Detection:

Monitor loop filter output—stable voltage indicates lock. Large variations indicate searching or loss of lock.

Capture Range:

PLL can only lock if initial frequency is within "capture range." If f_0 drifts too far, may need frequency sweep to re-acquire.

Alternatives to PLL

Method	Description	When to Use
Fixed Frequency	No tracking, fixed drive	Stable systems, low Q
Frequency Sweep	Periodically sweep through range	Testing, characterization
Peak Detector	Track amplitude maximum	Simpler than phase tracking
Self-Oscillation	Circuit sets own frequency	Simple, but less control

VIC Matrix Calculator Note: The VIC5 PLL module provides calculations for PLL component selection, including VCO tuning range, loop filter values, and expected tracking bandwidth. Use these calculations when implementing automatic resonance tracking.

Next: Harmonic Analysis →

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